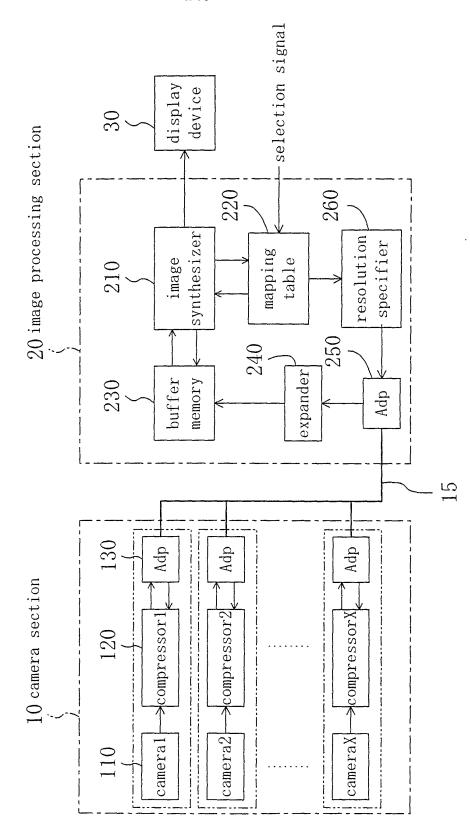
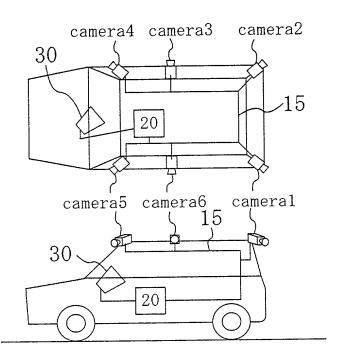
1/19



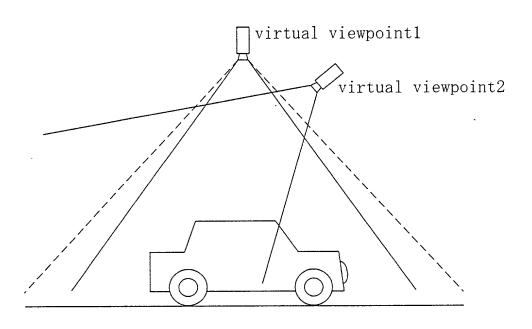
2/19

## FIG. 2

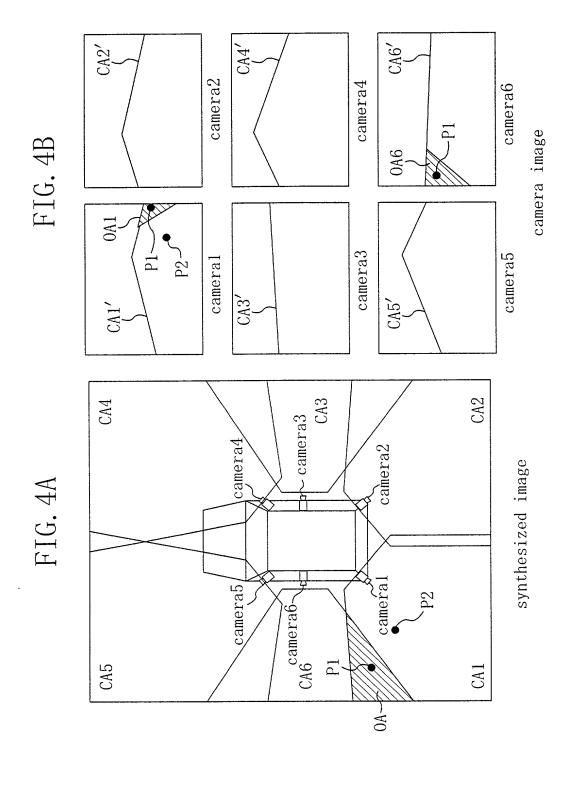


3/19

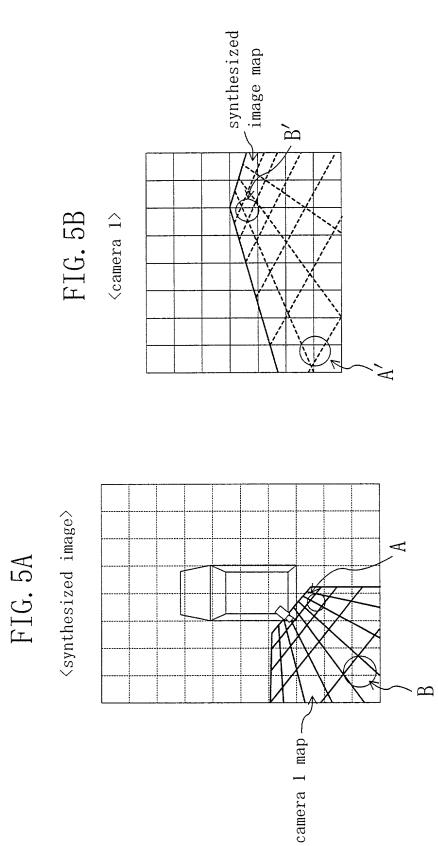
FIG. 3



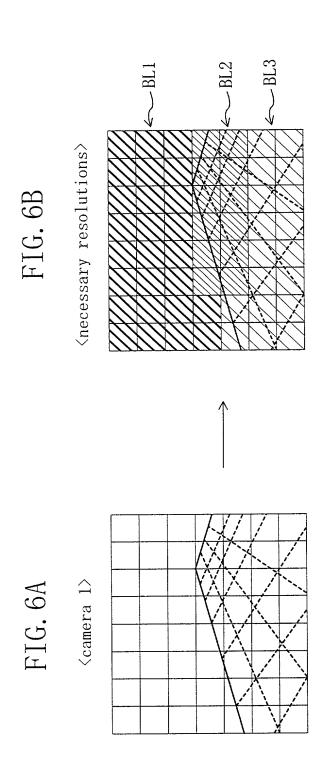
4/19



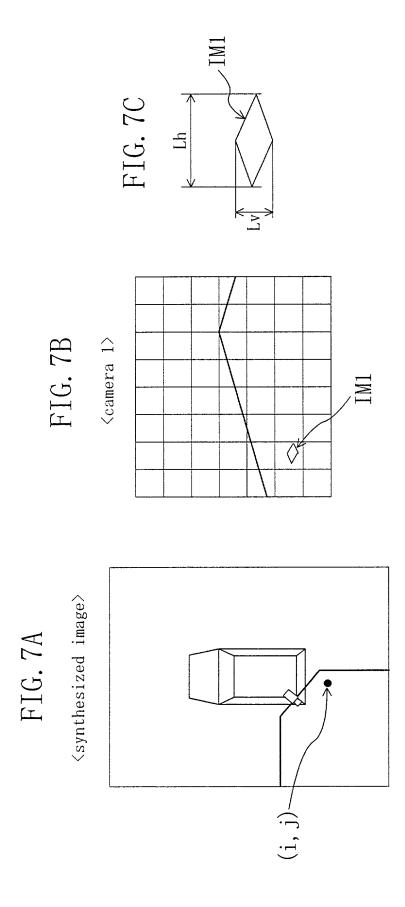
5/19



6/19



7/19



8/19

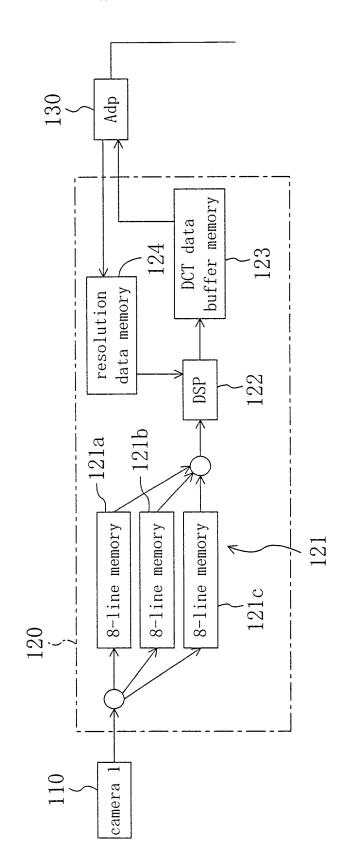
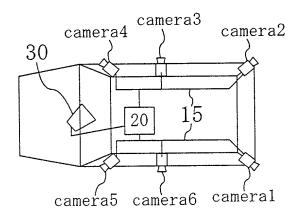


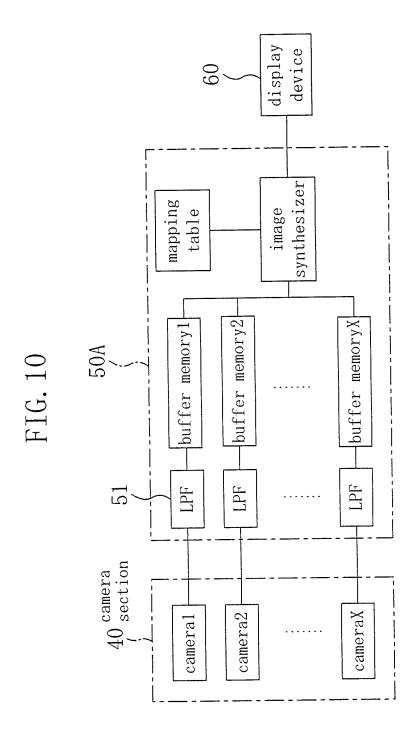
FIG. 8

9/19

## FIG. 9



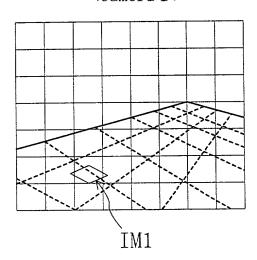
10/19



11/19

FIG. 11A

<camera 1>



## FIG. 11B

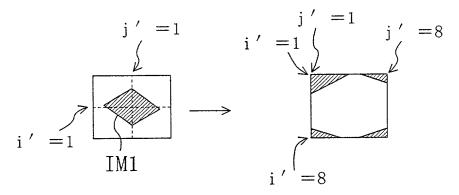
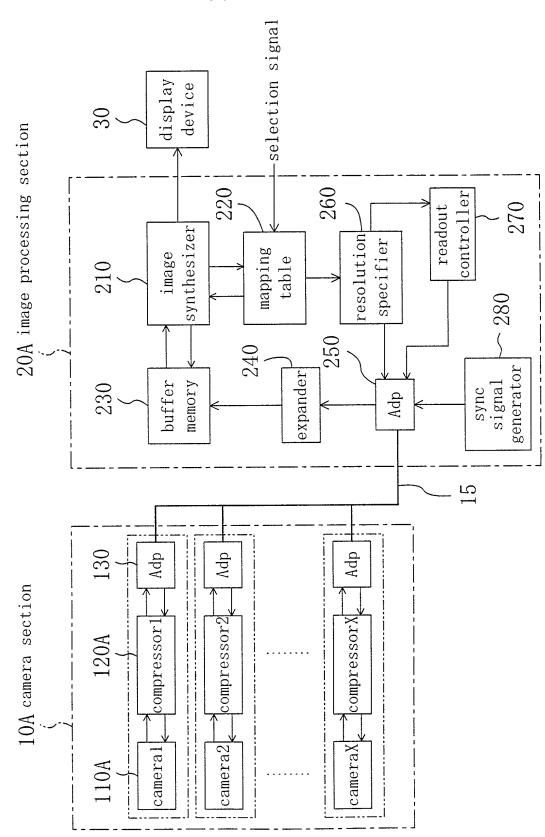


FIG. 12

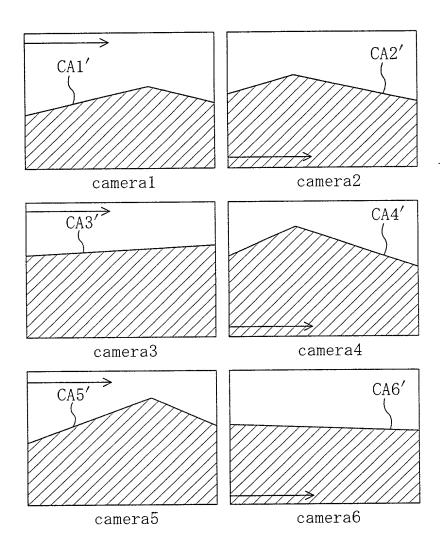
12/19



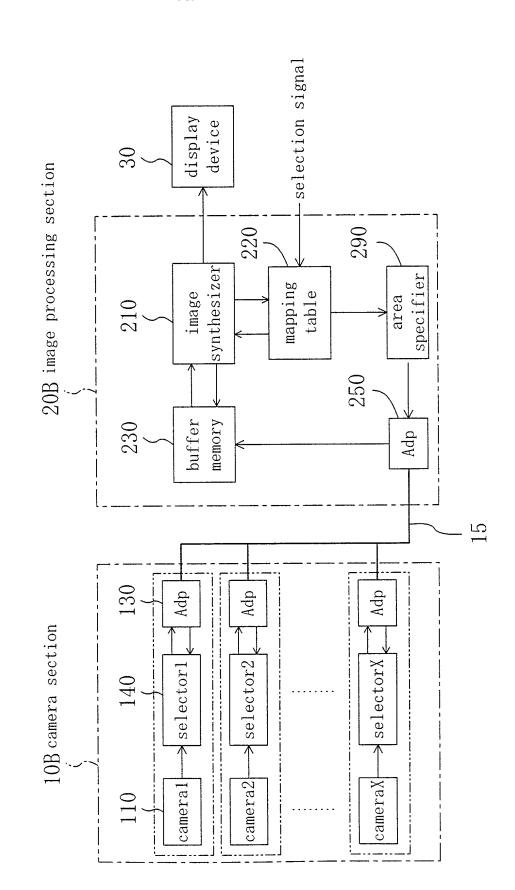
13/19 Adp buffer memory DCT data 123 125 area/resolution data sync 122 DSP and signals readout control FIG. 13 8-line memory 8-line memory 8-line memory 121 AD synchronization controller readout/

14/19

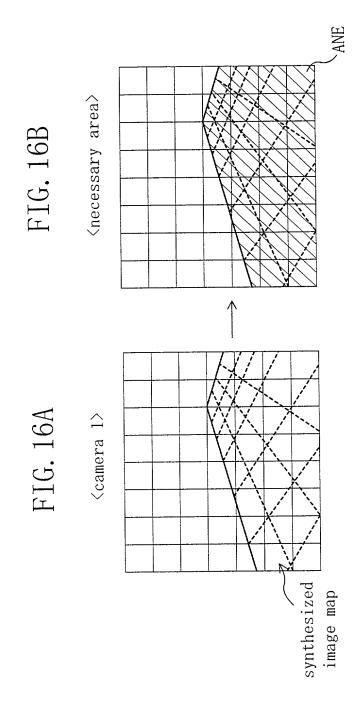
FIG. 14



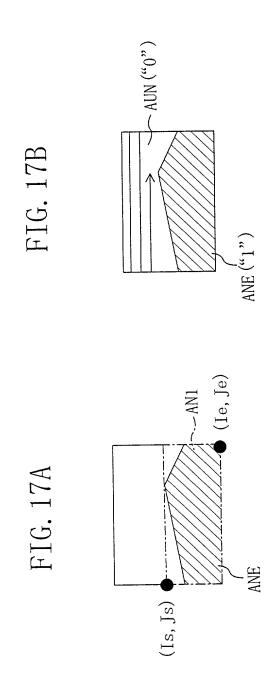
15/19



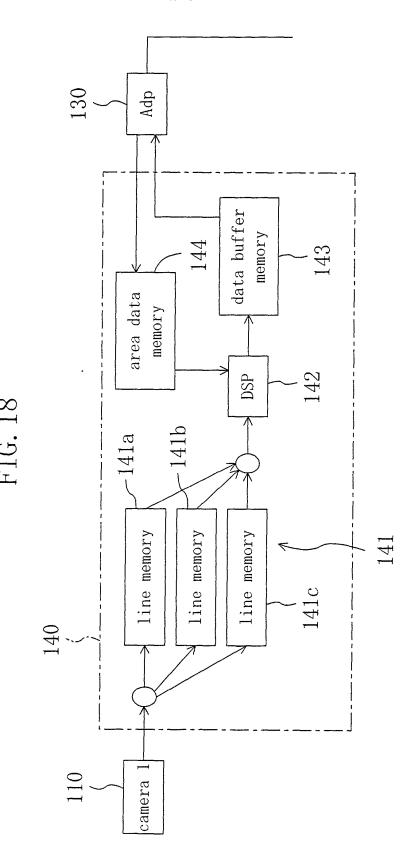
16/19



17/19



18/19



19/19

